Pulse pattern modulated strategy for harmonic current components reduction in three-phase AC-DC converters

Davari, Pooya; Zare, Firuz; Blaabjerg, Frede

Published in:
Proceedings of the 2015 IEEE Energy Conversion Congress and Exposition (ECCE)

DOI (link to publication from Publisher):
10.1109/ECCE.2015.7310497

Publication date:
2015

Document Version
Early version, also known as pre-print

Pulse Pattern Modulated Strategy for Harmonic Current Components Reduction in Three-Phase AC-DC Converters

Pooya Davari[†], Firuz Zare[‡], Frede Blaabjerg[†]

[†]Department of Energy Technology
Aalborg University, 9220 Aalborg, Denmark
pda@et.aau.dk, fbl@et.aau.dk

[‡]Danfoss Power Electronics A/S
6300 Gråsten, Denmark
fza@danfoss.com

***Abstract*—Generated harmonic current as a consequence of employing power electronics converter is known as an important power quality issue in distribution networks. From industry point of view complying with international standards is mandatory, however cost and efficiency are two other important features, which need to be considered in order to be competitive in the market. Therefore, having a flexibility to meet various requirements imposed by the standard recommendations or costumer needs is at most desirable. This makes the generated harmonic current mitigation a challenging task especially with three-phase diode bridge rectifier, which still is preferred in many power electronic systems. This paper addresses a novel current modulation strategy using a single-switch boost three-phase diode bridge rectifier. The proposed method can selectively mitigate current harmonics, which makes it suitable for different applications. The obtained results at experimental level verify and confirm the robustness of the proposed approach.**

Keywords—selective harmonic mitigation; three-phase rectifier; current control; modulation; electronic inductor;

I. INTRODUCTION

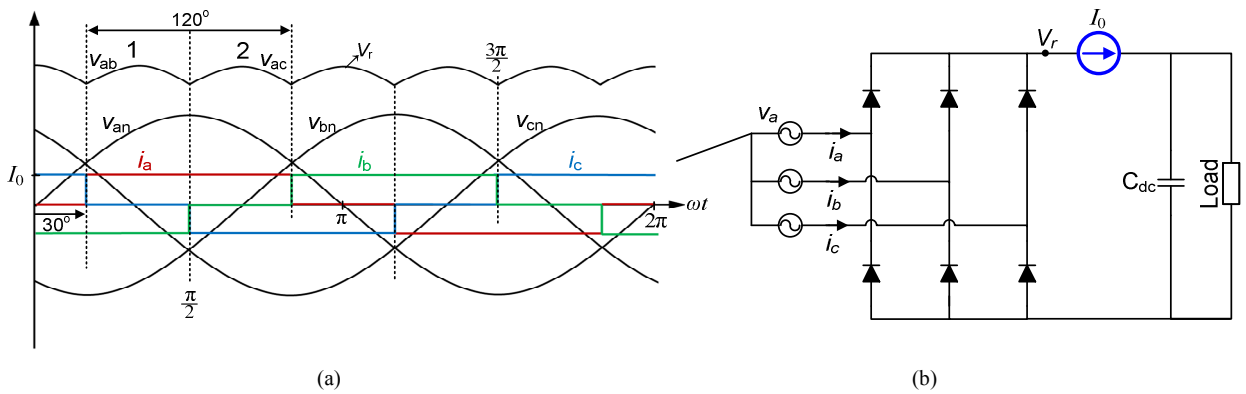
AC to DC conversion is an inevitable stage in most power electronic systems, but it is responsible for generating some line current harmonics especially if the conventional topologies such as six-pulse diode rectifier are employed. The level of generated current harmonics of this conversion stage is of significant importance as it can easily deteriorate the supply network quality [1]-[6]. Although the power electronic technology has brought new insight in many applications, however controlling their generated harmonics at certain levels is not achievable without additional cost and circuitry.

The basic topology for AC to DC conversion has started by utilizing a diode bridge rectifier due to many reasons such as simplicity, reliability, robustness, and being cost-effective compared to other complex systems such as active front end systems. However, the diode rectifiers impose a higher level of line current harmonics. Over the past years, many approaches have been studied and introduced from absolutely passive up to fully active methods [1], [4]-[10]. A majority of these methods have targeted pure sinusoidal waveform generation, and as a consequence cost and complexity have been significantly increased. Of course having a low Total Harmonic Current Distortion (THD_i) improves the system efficiency but this is of interest for specific applications such as space and airborne industry, where the cost of the power converter is not the main concern. But with most applications such as industrial Adjustable Speed Drives (ASDs), switch mode power supplies, home appliances and etc, the key of success is to perform a trade-off between efficiency and cost since many manufacturers are competing in the market. Therefore, as long as the power electronic system complies with the recommended standards there is no need to obtain a pure sinusoidal current waveform. Moreover, due to the cost, power density and components limited power ratings many of the prior-art approaches are not applicable at medium and high power levels.

With the rapid growth of power electronics applications, the standard recommendations such as IEC61000 are continuously updating and becoming more stringent. In addition, the demands on various power level and costumer needs are extending. These bring the absolute interest of having a flexible system which can be adapted with varied situation as it can reduce the cost of the system significantly. This paper proposes a novel current modulation strategy to reduce low order harmonic current components. The objective of the proposed method is to address a flexible selective harmonic mitigation technique suitable for various applications. Due to its simplicity this strategy is applied to a single-switch boost three-phase rectifier topology and verified through different practical experimental cases.

This paper is structured as follows. Section II provides detailed analysis of selective harmonic mitigation using the proposed current modulation strategy. In Section III, practical design considerations with respect to the boost inductor and modulation signal generation are pointed out. The obtained experimental results that are summarized in Section IV validate the performance of the proposed method. Section V recalls a brief overview on the possible future development. Finally, concluding remarks are given in Section VI by highlighting the main achievements and providing suggestions for further studies.

978-1-4673-7151-3/15/$31.00



(a) (b)

Fig. 1. Circuit diagram of a three-phase diode rectifier with a controlled DC-link current, (a) ideal three-phase input currents, (b) systems schematic.

II. Proposed Current Modulation Strategy

A. Principle of the Proposed Method

In order to understand the basic principle of the proposed method, let's first consider the circuit diagram depicted in Fig. 1. As it ca n be seen, the current source at the DC-link side of the rectifier draws a constant current which is equal to I_0. Therefore, the input current will be a square-wave with 120 degrees conduction due to the fact that at each instant of time only two phases conduct and circulate DC-link current through the main supply. Due to the nature of a three-phase system (120^o phase shift), the corresponding phase shift for any triple harmonic would be a multiple of 360^o and since the currents at each instant are identical with opposite amplitude, the sum of line currents i_a, i_b, and i_c is zero at all instants of time, which makes them to be free from triple harmonics in a balanced system. The currents are also void of even harmonics because of the half-wave symmetry of the waveforms which as a matter of fact makes the most prominent harmonics in this system to be the fifth, seventh, eleventh, and thirteenth [11].

The proposed idea is based on adding (or subtracting) phase-displaced current levels to the square-wave current waveform in order to manipulate the current harmonic components [12]. To keep the above mentioned properties (free of triple and even harmonics) the new added pulse should be repeated 1/6 of the period. For instance, Fig. 1 depicted two sectors of 1 and 2, where at each sector i_a is circulated through one of the other phases current. Now, if the new level is added at sector 1 it should be exactly repeated in sector 2 (see Fig. 2(a)). This means that the frequency of the added pulse at the DC-link should be six times of the fundamental frequency so it can be repeated at each phase current.

Fig. 2(a) illustrates detailed analysis of the proposed idea for only one new level added to a constant square wave. As can be seen the proposed current waveform is comprises of three square-wave signals with different magnitudes and pulse widths. The first current waveform has the magnitude of I_0 with the conduction phase angle of 30^o, which is defined based on the normal operating modes of a three-phase diode rectifier and the conduction phase angle cannot be altered. The second current waveform has the magnitude of I_1 with the conduction phase angle of α_1. The third current waveform has the magnitude of I_1 but with a different conduction phase angle (α_{11}). These current waveforms can be analyzed based on a periodic square-wave Fourier series in which the fundamental input current magnitude and its harmonics can be calculated as follows:

$$i_n = \frac{4}{n\pi}\left[I_0\cos(n30) + I_1\cos(n\alpha_1) - I_1\cos(n\alpha_{11})\right] \qquad (1)$$

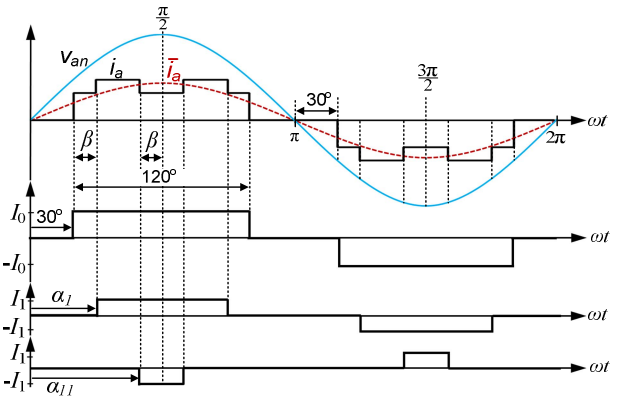
Equation (1) shows that the fundamental current can be defined by selecting the variables I_0, I_1, α_1 and α_{11} but a main consequence will be on harmonic magnitudes. According to the line current waveform depicted in Fig. 2(a) the following condition should be valid:

$$\alpha_{11} = \frac{\pi}{2} - \beta, \quad where \quad \beta = \alpha_1 - \frac{\pi}{6} \qquad (2)$$

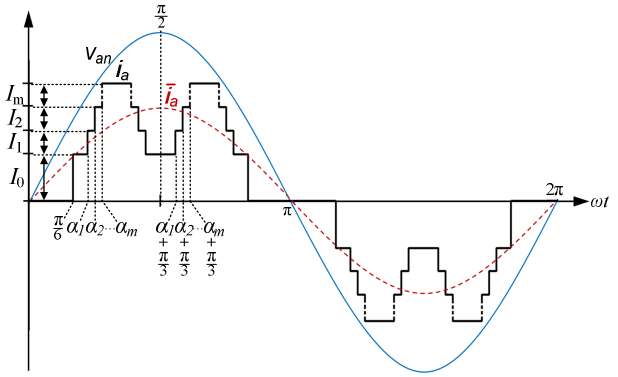
Considering (1) and (2) and having α_1 and α_{11} as the switching angles, up to two selected low order harmonics (i_{hth} and i_{jth}) can be cancelled out. The mathematical statement of these conditions can be expressed as (3). This is a system of three transcendental equations with three unknown variables I_0, I_1, α_1

$$\begin{aligned}
i_1 &= \frac{4}{\pi}\left[I_0\cos\left(\frac{\pi}{6}\right) + I_1\cos(\alpha_1) - I_1\cos\left(\frac{2\pi}{3} - \alpha_1\right)\right] = M_a \\
i_{hth} &= \frac{4}{h\pi}\left[I_0\cos\left(h\frac{\pi}{6}\right) + I_1\cos(h\alpha_1) - I_1\cos\left(h\left(\frac{2\pi}{3} - \alpha_1\right)\right)\right] = 0 \\
i_{jth} &= \frac{4}{j\pi}\left[I_0\cos\left(j\frac{\pi}{6}\right) + I_1\cos(j\alpha_1) - I_1\cos\left(j\left(\frac{2\pi}{3} - \alpha_1\right)\right)\right] = 0
\end{aligned} \qquad (3)$$

The proposed method can be further extended to a multilevel current waveform. Fig. 2(b) illustrates a generalized pulse modulated current waveform, where m is the number of



(a)



(b)

Fig. 2. Detailed analysis of the proposed current modulation technique with: (a) one new added level, (b) generalized *m*-level pulse modulated.

switching angles. By extending (3) and using Fourier series, the amplitude of any odd n^{th} harmonic of the stepped current waveform can be expressed as:

$$i_n = \frac{4}{\pi}\left(I_0\cos\left(n\frac{\pi}{6}\right)+\frac{1}{n}\sum_{k=1}^{m}\left[I_k\cos(n\alpha_k)-I_k\cos\left(n\left(\frac{2\pi}{3}-\alpha_k\right)\right)\right]\right) \quad (4)$$

According to Fig. 2(b), α_1 to α_m must satisfy the following condition:

$$\frac{\pi}{6}<\alpha_1<\alpha_2<\alpha_3<\cdots<\alpha_m<\frac{\pi}{2} \quad (5)$$

From (5) it can be seen that the degree of freedom in manipulating the current waveform is only 60°, which makes the control of the harmonic components a difficult task. Therefore, to give more flexibility to (4) the new added levels should not necessarily have same amplitude. In addition, the amplitude could be positive or negative, which totally depends on the targeted harmonics and the desired modulation index M_a (fundamental harmonic content). As the equations are nonlinear, numerical solutions are required to find proper values for these variables.

B. Optimum Harmonic Reduction

To target more harmonic components the number of the current levels need to be increased, but on the other hand it reduces the feasibility of practical implementation since the new added levels and switching angles depends on the tracking performance of the power electronics unit and its controller. Therefore, in order to keep the number of the added current levels to minimum while obtaining desirable outcome an optimization needs to be performed. The basic principle of the applied optimization is to consider the maximum permissible harmonic levels allowed by the application or the grid code. In other word, instead of fully nullifying, the harmonic components could be reduced to acceptable levels by adding suitable constraints (L_n) to the set of the above mentioned equations. The problem is now described as an optimization function (F_n) that searches a set of α_m and I_m values over the allowable intervals.

$$\begin{aligned} F_1 &= M_a - |i_1| \le L_1 \\ F_n &= \frac{|i_n|}{|i_1|} \le L_n, \quad \text{where} \quad n = 5,7,11,13,\cdots \end{aligned} \quad (6)$$

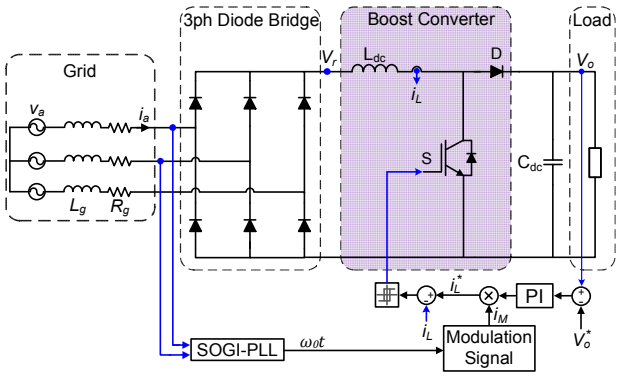
Based on (6) an objective function needs to be formed to obtain a minimum error. The objective function (F_{obj}) plays an important role in leading the optimization algorithm to the suitable set of solution. Here F_{obj} is formed based on squared error with more flexibility by adding constant weight values (w_n) to each squared error function [13]. The value of the w_n in the objective function prioritized the included functions as follows:

$$F_{obj} = \sum w_n \cdot (F_n - L_n)^2, \quad \text{where} \quad n = 1,5,7,11,13,\cdots \quad (7)$$

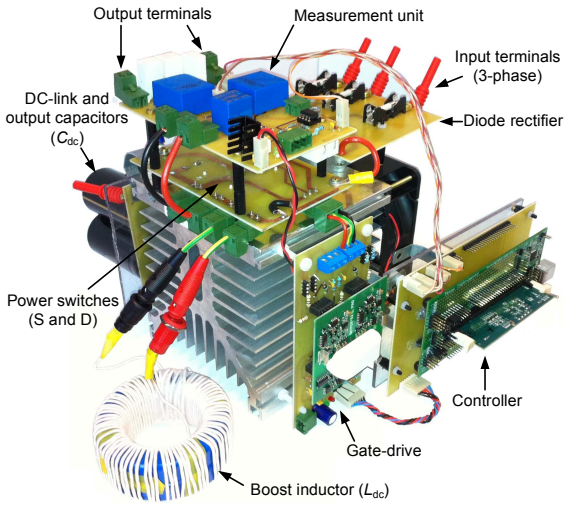
III. Implementation Details and Hardware Setup

To control the DC-link current shape and magnitude following the waveforms shown in Fig. 2, a boost converter topology based on electronic inductor [12], [14]-[18] concept is employed. Fig. 3 depicts the overall system structure and the implemented hardware setup. Using the conventional boost topology has the advantage of boosting the output DC voltage which is suitable when the DC-link is fed to an inverter. Moreover, as the DC-link current is controlled based on the load power it has the advantage of keeping the THD_i independent of load profile. The reference tracking performance of the current controller has an important role in the harmonic mitigation, and employing a fast current control method like hysteresis or dead-beat are of much interest.

Fig. 3(b) shows the implemented prototype. Here, one SEMIKRON-SKD30 was used as a three-phase bridge rectifier and one SEMIKRON-SK60GAL125 IGBT-diode module is employed in boost topology. A Texas Instrument TMSF28335



(a)



(b)

Fig. 3. The implemented three-phase AC-DC system with the proposed selective harmonic elimination method, (a) overal system structure, (b) photograph of the implemented hardware setup.

is used for control purposes and LEM current and voltage transducers are used as measurement unit.

To synchronize the current controller with the grid a Second-Order Generalized Integrator (SOGI) based phase locked loop (PLL) system is adopted [19]. As Fig. 3(a) depicted, for the simplicity, one line-to-line voltage is fed to the PLL and therefore the result will have 30° phase shift regarding to the phase voltage, which should be corrected within the reference current generator algorithm. In order to obtain a discrete-time integrator for PLL and PI controller, the trapezoidal discretization method is used.

A. Boost Inductor

Selection of the boost inductor is a challenging task as it contributes to the system loss, power density and current ripple. To better understand this, the inductor current in a steady-state Continuous Conduction Mode (CCM) is analyzed. Here the switching frequency is considered to be high enough so that the rectified voltage and output voltage are constant during one switching cycle. Therefore, the inductor value can be calculated as,

$$L_{dc} = \frac{V_o D(1-D)}{f_{sw}\Delta I_{L,pk-pk}} \quad where \quad f_{sw} = \frac{1}{T_{sw}} = \frac{1}{T_{on}+T_{off}} \tag{8}$$

where V_o is the output voltage, f_{sw} is the switching frequency, $\Delta I_{L,pk\text{-}pk}$ is the peak to peak inductor current ripple and D is the steady-state duty cycle of the boost converter. Using (13) the minimum required switching frequency (f_{sw}) can be selected by considering the maximum peak to peak inductor current ripple ($D = 0.5$) as,

$$f_{sw} \geq \frac{V_o}{4L_{dc}\Delta I_{L,pk-pk,\max}} \tag{9}$$

Following (8) and (9) the optimum switching frequency can be selected by making a tradeoff among the system efficiency, size and cost [21]. For example the system efficiency can be optimized by minimizing the switching frequency by allowing more ripple current for high power applications and it will result in lower switching losses.

As mentioned before the THD_i can be independent of the load profile. Equation (8) can be rewritten based on the output average current as

$$L_{dc} = \frac{V_o D(1-D)^2}{f_{sw} k_{ripple} I_{out}} \text{ where } \quad k_{ripple} = \frac{\Delta I_{L,pk-pk}}{I_L} = \frac{\Delta I_{L,pk-pk}(1-D)}{I_{out}} \tag{10}$$

with k_{ripple} being the ripple factor, I_L the average inductor current and I_{out} the average output current. Hence, keeping the ripple factor as a constant value will make the input current quality independent of the load profile. However, careful selection of the ripple factor is needed as it has direct relation with the ripple current, which as stated in (9) can affect the inductor size, system efficiency and cost [21].

B. Modulation Signal

As Fig. 3(a) illustrates the reference current is formed by multiplying the voltage controller output by a pre-programmed modulation signal. Fig. 4 depicts the basic concept in generating the modulation signal (i.e., i_M) following Fig. 2(a). As it can be seen, i_M can be generated based on the sum of absolute values of three-phase input currents. The illustrated switching parameters (i.e., I_0, I_1 and α_1) at both grid side and DC-link currents helps to better understand this relation. As it can be seen the period of the modulation signal i_M is 1/6 of the input currents i_{abc}. Therefore, the simplest way to generate and synchronize the modulation signal inside the controller is to compare it with a sinusoidal signal (i.e., $|\sin(3\omega_0 t)|$) using the PLL estimated angular frequency (ω_0). Comparing the switching angles with the sinusoidal waveform yields

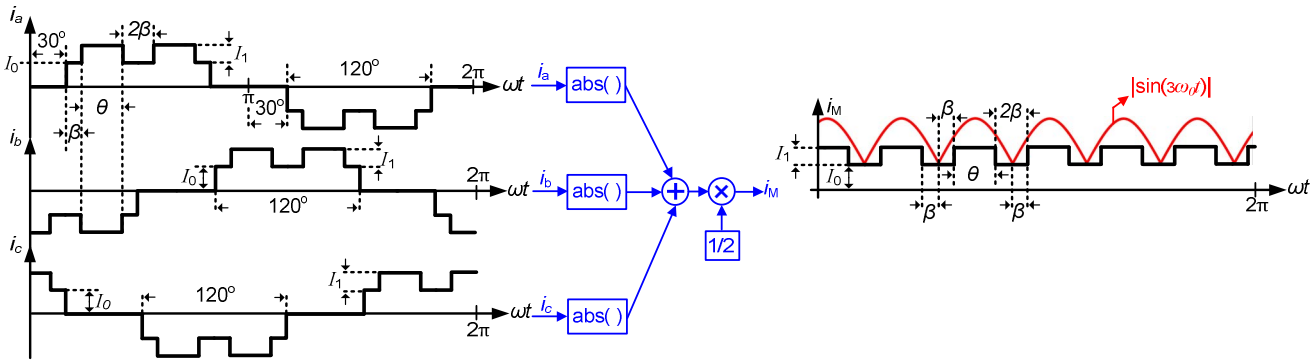


Fig. 4. Synthesis of the modulation signal (i.e., i_M) at the DC-link based on three-phase input currents.

$$
\begin{cases}
\alpha_1 < \alpha_{11}: \\
\quad \begin{cases} if\left(\left|\sin(3\omega_0 t)\right| > \sin(3\beta)\right) \\ i_M = I_0 + I_1 \\ else \\ i_M = I_0 \end{cases} \\
\alpha_1 > \alpha_{11}: \\
\quad \begin{cases} if\left(\left|\sin(3\omega_0 t)\right| > \sin(3\beta)\right) \\ i_M = I_0 - I_1 \\ else \\ i_M = I_0 \end{cases}
\end{cases} \tag{11}
$$

Here, based on the fact that the proposed method is adding or subtracting phase-displaced current levels, two conditions have been considered, which results in different modulation signals. It can be known from Fig. 2(a) that adding a phase-displaced current level requires to have $\alpha_1<\alpha_{11}$. However to reduce a specific set of harmonic components phase displaced current level needs to be subtracted. Therefore, for those situations α_1 should be set above α_{11} ($\alpha_1>\alpha_{11}$). The above equation can easily be extended to multi-level situation by applying (11) to each switching parameters and summing up the corresponding modulation signals.

IV. Experimentatal Results

In this section the circuit operation and the proposed current modulation scheme are verified through different experiments using the implemented prototype (Fig. 3(b)). Here the flexibility of the proposed method by targeting different set of harmonic components is illustrated. The system parameters are listed in Table I.

For the first case adding one current level to the DC-link current was considered to target two low order harmonics. Hence, the cancellation of 7th and 13th harmonic orders have been considered by solving (3) using MATLAB function – "fsolve". Fig. 5 illustrates the obtained results. As it can be the

TABLE I.
Parameters of the System

Symbol	Parameter	Value
v_{abc}	Grid phase voltage	220 V_{rms}
f_g	Grid frequency	50 Hz
L_g, R_g	Grid impedance	0.18 mH, 0.1 Ω
L_{dc}	DC link inductor	2 mH
C_{dc}	DC link capacitor	470 µF
V_o	Output voltage	700 V_{dc}
K_p, K_i	PI controller (Boost converter)	0.01, 0.1
HB	Hysteresis band	2 (A)
P_o	Output power	≈3 kW

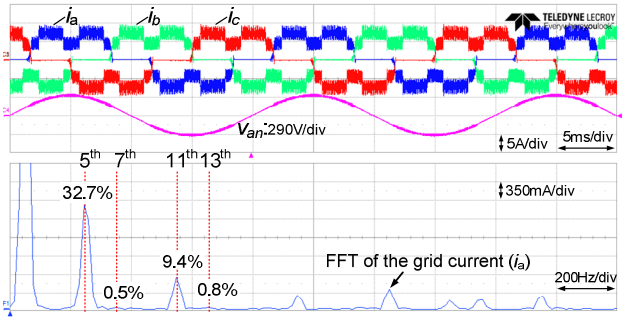


Fig. 5. Experimental results for 7th and 13th harmonics cancellation using hysteresis current control at V_o = 700 V_{dc} and P_o ≈ 3kW: (a) Two-level three-phase input currents, (b) Fast Fourier Transform (FFT) of the input current (i_a) [with I_0 = 1, I_1 = 0.618, α_1= 42°].

consequence of canceling 7th and 13th harmonics is the increase of the 5th harmonic order. In fact, reducing 7th harmonic increases 5th harmonic and vice versa, which results in higher THD_i comparing with the conventional square-wave case. This can be understood by solving (3) for these harmonic orders. The solution for eliminating 5th harmonic requires to select $60^o<\alpha_1<90^o$ which is in contrary to 7th harmonic where $34^o<\alpha_1<60^o$ making it impossible to target these two harmonics at the same time.

A proper selection of the harmonics to be reduced or eliminated depends on the application needs. To exemplified,

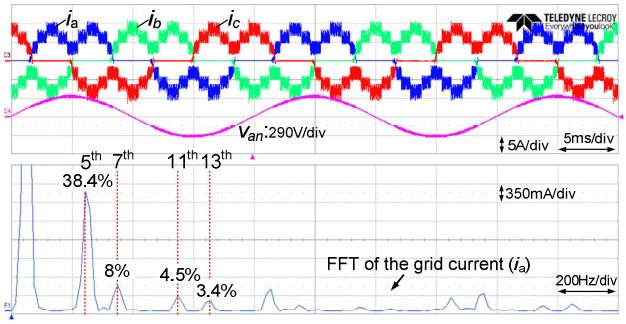


Fig. 6. Experimental results for 7th , 11th and 13th harmonics cancellation using hysteresis current control at V_o = 700Vdc and $P_o \approx$ 3kW: (a) Two-level three-phase input currents, (b) Fast Fourier Transform (FFT) of the input current (i_a) [with $I_0 = 1$, $I_1 = 0.7328$, $\alpha_1 = 38.3^o$, $I_2 = 0.7328$, $\alpha_2 = 51.5^o$].

TABLE II.
COMPARATIVE EXPERIMENTAL RESULTS AT OUTPUT POWER LEVEL OF 3 KW

Harmonic Mitigation Strategy	Harmonic Distribution and THD_i (%)				
	$i_{a,5}/i_{a,1}$	$i_{a,7}/i_{a,1}$	$i_{a,11}/i_{a,1}$	$i_{a,13}/i_{a,1}$	THD_i
7th and 13th harmonic cancellation	32.7	0.5	9.4	0.8	35.3
7th , 11th and 13th harmonic cancellation	38.4	8	4.5	3.4	41.1
Conventional method (square-wave)	21	13	8.9	7	29

in the second case adding two levels to the square-wave current is considered following (4) and 7th, 11th and 13th harmonic orders are targeted to be half of their values comparing to the square-wave current. Here, following (7) an optimization needs to be performed, which has been done using a MATLAB genetic optimization algorithm. It is important to apply the suitable restrictions following (5) and (6). As Fig. 6 shows the three harmonic orders of 7th, 11th and 13th have been reduced which as explained before results in increase of the 5th harmonic. Table II summarizes the obtained results based on the targeted harmonic orders and THD_i for both the proposed and the conventional square-wave methods. As can be seen for both cases the obtained results slightly differ from what expected which is due to the presence of grid impedance, and consequently affects the calculated angles.

Finally, the start-up and shut-down dynamic behavior of the implemented system are illustrated in Fig. 7. For the start-up case the input voltage is already applied, the load current is flowing and boost converter is in the off-state. Turning on the DC-DC converter makes the controller to start the pulse pattern modulation at input current i_a and changes the output voltage V_o from 515 V_{dc} to 700 V_{dc} without any large overshoot (Fig. 7(a)). The symmetrical pulse patterns on the input current after 100 ms validate the PLL settling time. At shut-down phase of operation the control circuit permanently turns off the IGBT switch so it stops the current modulation and the output voltage drops to 515 V_{dc} (Fig. 7(b)).

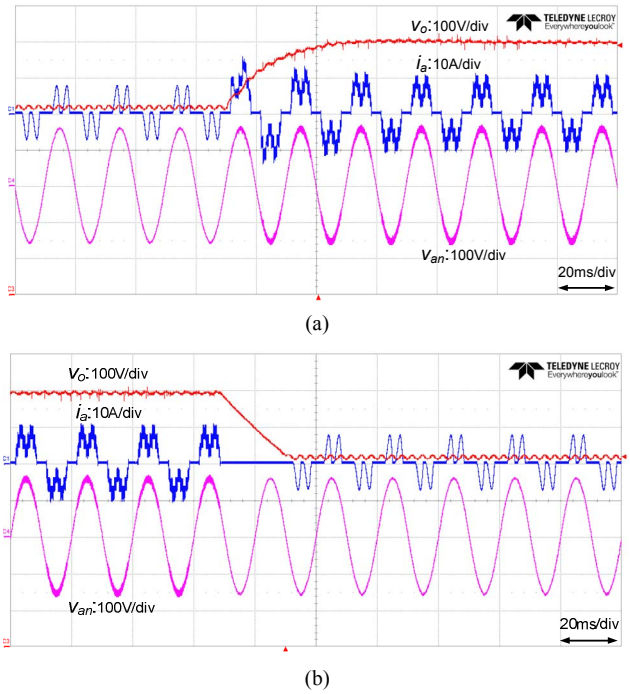


Fig. 7. Measured dynamic behavior of input current ia and output voltage V_o at (a) startup and (b) shutdown at the nominal operating conditions.

V. FUTURE DEVELOPMENT

The proposed concept gives the possibility to eliminate various sets of harmonic components in a three-phase diode rectifier based on electronic inductor concept. Therefore, based on the application requirement employing the proposed method can further improve the input current quality by reducing the low order harmonics. However, as stated before, targeting 5th and 7th orders harmonic simultaneously solely based on a single unit system is impossible. In this section, one of the possible solutions based on combination of nonlinear loads [20] are briefly discussed.

Here, the proposed method is applied to a multi-pulse rectifier system [10]. Fig. 8(a) illustrates the application of the proposed concept in a 12-pulse rectifier topology with a common DC-bus. Basically, the 12-pulse arrangement eliminates the 5th, 7th, 17th and 19th harmonic orders. The improved input current harmonic distortion for a 12-pulse rectifier system depending on the output power level varies between 10 % < THD_i < 15 %. Hence, employing the proposed current modulation strategy can further improve the input current quality by targeting the remaining 11th, 13th, 23th and 25th harmonic orders. The obtained results in Figs. 8(b) and 8(c) show that the new 12-pulse rectifier system obtained $THD_i \approx$ 3.8 %. In fact, the only remaining 35th and 37th harmonics imply that applying the proposed method improves the performance of a conventional 12-pulse rectifier system to be comparable with a conventional 24-pulse rectifier system. Moreover, the output voltage can be increased to higher voltage levels using the boost topology; this is beneficial when the DC-link voltage is fed to an inverter. Unlike the

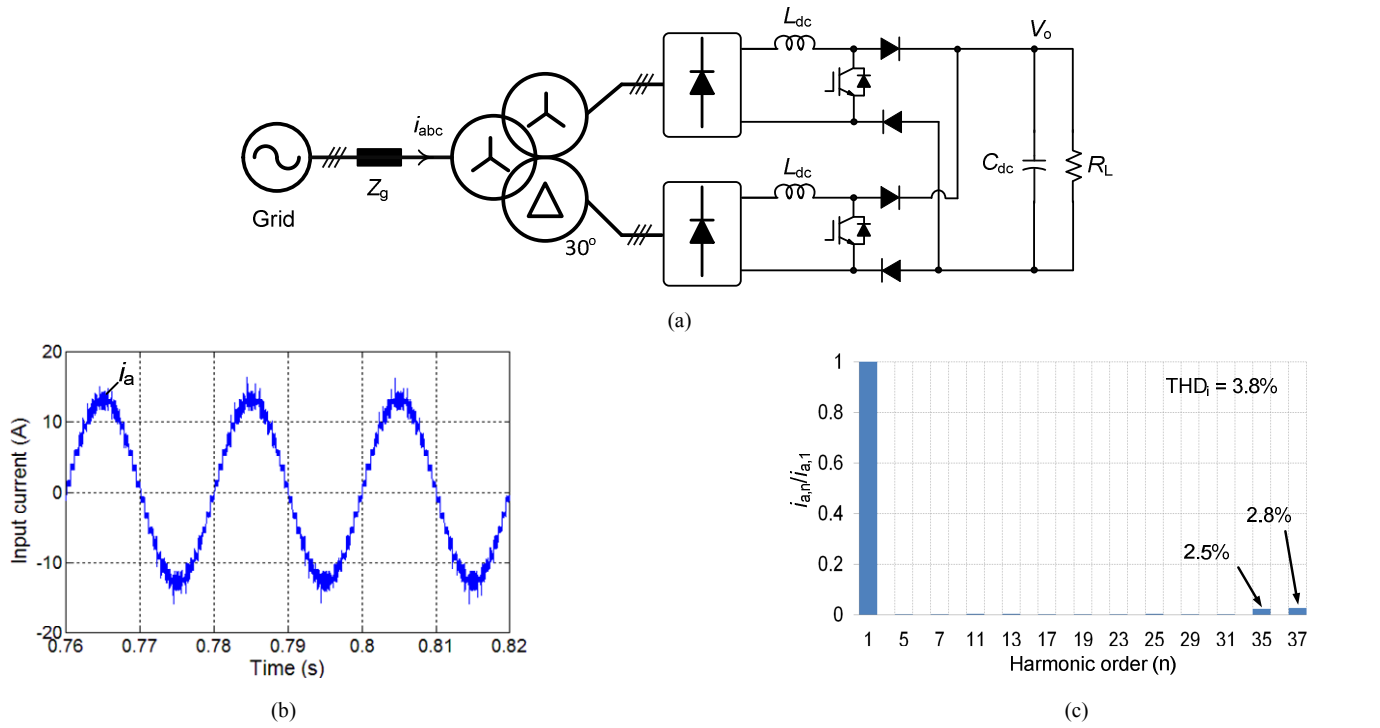


Fig. 8. Extension of conventional 12-pulse rectifier system based on proposed current modulation strategy: (a) circuit schematic, (b) simulated input current waveform (i_a) and (c) input current FFT at V_o = 700 V_{dc} and at P_o = 6 kW.

conventional multi-pulse rectifier systems which the performance of the system is dependent of the load profile, applying the proposed concept can maintain the input current THD$_i$ regardless of the output power variation.

VI. Conclusion

In this paper a novel current modulation technique has been proposed for a three-phase rectifier with an electronic inductor at the DC-link side. The proposed method modulates the DC-link current to control the fundamental current and to reduce the selected line current harmonics. Moreover, calculations of the optimum switching patterns have been conducted based on applying the minimum number of current levels. A main advantage of the proposed method is that the relative values of harmonics with respect to the fundamental value remain constant regardless of load profile variation. Applying the proposed method to other configurations such as 12-pulse rectifier can significantly improves THD$_i$ comparative to an 24-pulse rectifier. The performance of the proposed method can be improved by increasing the number of the levels in order to obtain optimum solutions for low order harmonics which completely depends on the switching frequency and inductor size.

References

[1] D. Kumar and F. Zare, "Analysis of harmonic mitigations using hybrid passive filters," in *Proc. of PEMC*, 2014, pp. 945-951.

[2] J.W. Gray and F. J. Haydock, "Industrial power quality considerations when installing adjustable speed drive systems," *IEEE Trans. Ind. Appl.*, vol. 32, no. 3, pp. 646-652, May/Jun 1996.

[3] F. Zare, "Harmonics issues of three-phase diode rectifiers with a small DC link capacitor," in *Proc. of PEMC*, 2014, pp. 912-917.

[4] C. Klumpner, F. Blaabjerg, and P. Thogersen, " Alternate ASDs: evaluation of the converter topologies suited for integrated motor drives," *IEEE Ind. Appl. Mag.*, vol. 2, no. 2, pp. 71-83, 2006.

[5] J. W. Kolar and T. Friedli, "The Essence of Three-Phase PFC Rectifier Systems - Part I," *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 176-198, Jan. 2013.

[6] B. Singh, B. N. Singh, A. Chandra, K. Al-Haddad, A. Pandey, and D. P. Kothari, "A review of three-phase improved power quality AC-DC converters," *IEEE Trans. Ind. Electron.*, vol. 51, pp. 641-660, 2004.

[7] M. Liserre, F. Blaabjerg, and S. Hansen, "Design and control of an LCL-filter-based three-phase active rectifier," *IEEE Trans. Ind. Appl.*, vol. 41, no. 5, pp. 1281-1291, 2005.

[8] M. Liserre, A. Dell'Aquila, and F. Blaabjerg, "An overview of three-phase voltage source active rectifiers interfacing the utility," in *Proc. of Power Tech Conf.*, 2003, vol. 3, pp. 1-8.

[9] H. Akagi, "Modern active filters and traditional passive filter," Bulletin of the polish academy of sciences technical sciences, vol. 54, 2006.

[10] H. Akagi and K. Isozaki, "A hybrid active filter for a three-phase 12-pulse diode rectifier used as the front end of a medium-voltage motor drive," *IEEE Trans. Power Electron.*, vol. 27, no. 1, pp. 69-77, Jan. 2012.

[11] A. M. Trzynadlowski, Introduction to modern power electronics: John Wiley & Sons, 2010.

[12] F. Zare, "A novel harmonic elimination method for a three-phase diode rectifier with controlled DC link current," in *Proc. of PEMC*, 2014, pp. 985-989.

[13] L.G. Franquelo, J. Napoles, R.C.P. Guisado, J.I. Leon, and M.A. Aguirre, "A flexible selective harmonic mitigation technique to meet grid codes in three-level PWM converters," *IEEE Trans. Ind. Electron.*, vol.54, no.6, pp.3022-3029, Dec. 2007.

[14] K. Mino, M. L. Heldwein, and J. W. Kolar, "Ultra compact three-phase rectifier with electronic smoothing inductor," in *Proc. of APEC*, 2005, pp. 522-528.

[15] J. Salmon and D. Koval, "Improving the operation of 3-phase diode rectifiers using an asymmetrical half-bridge DC-link active filter," in *Proc. of IAS Annual Meeting*, 2000 vol. 4, pp. 2115-2122.

[16] H. Ertl and J. W. Kolar, "A constant output current three-phase diode bridge rectifier employing a novel "Electronic Smoothing Inductor"," *IEEE Trans. Ind. Electron.,* vol. 52, pp. 454-461, 2005.

[17] C. Galea and L. Asiminoaei, "New topology of electronic smoothing inductor used in three phase electric drives," in *Proc. of EPQU*, 2011, pp. 1-6.

[18] P. J. Grbovic, P. Delarue, and P. Le Moigne, "A Novel Three-Phase Diode Boost Rectifier Using Hybrid Half-DC-Bus-Voltage Rated Boost Converter," *IEEE Trans. Ind. Electron.*, vol. 58, no. 4, pp. 1316-1329, 2011.

[19] M. Ciobotaru, R. Teodorescu, and F. Blaabjerg, "A New Single-Phase PLL Structure Based on Second Order Generalized Integrator," in *Proc. of PESC*, 2006, pp. 1-6.

[20] S. Hansen, P. Nielsen, and F. Blaabjerg, "Harmonic cancellation by mixing nonlinear single-phase and three-phase loads," *IEEE Trans. Ind. Appl.*, vol. 36, no. 1, pp. 152-159, Jan/Feb 2000.

[21] T. Nussbaumer, K. Raggl, and J.W. Kolar, "Design Guidelines for Interleaved Single-Phase Boost PFC Circuits," IEEE Trans. Ind. Electron., vol.56, no.7, pp.2559-2573, July 2009.